

Exact analysis of a simple class E circuit version for device characterization purposes

Pilar Molina Gaudio, Carlos Bernal, Arturo Mediano

Departamento de Ingeniería Electrónica y Comunicaciones

Universidad de Zaragoza

E-mail: pimolina@ieee.org

Abstract— The mathematical exact analysis of a simple class E high-efficiency switching mode tuned power amplifier [1] is performed. The simple network only contains one capacitor and one inductor. Switch duty-cycle and Q , cannot be chosen independently, and thus this circuit is only of interest for applications in which a high harmonic content in the load is permitted. In this paper, this circuit is used as a test bench for extracting, with no need for optimization, the parameters of a simple FET output port model in high frequency switching conditions. This method is a quick way to predict if a transistor will be useful in a class E application. Experimental measurements showing good agreement with theoretical results are presented.

I. INTRODUCTION

Figure 1a and 1b present two equivalent circuits of a simple version of the class E network [1]. In this case, only one inductor and one capacitor are needed. The capacitor is the parallel combination of the device's output capacitance and an external capacitor. The load resistance in fig.1b is the equivalent load resistance of the RF transformer and the series loss resistance of the coil. The active device is driven at the operating frequency, f , and it is considered to be acting as a switch. This network has the following limitations:

- 1) D (duty-cycle) of the driving signal and loaded Q are not independent.
- 2) Current through the load is not a sinusoid and the harmonic output content of the output signal can be high, so the application range of this particular topology is limited.

In this paper, an analytical description of this circuit is obtained and applied to develop a parameter extraction method for characterization purposes. For this particular application this version of the class E amplifier is useful for the following reasons:

- 1) The harmonic content of the output signal is irrelevant.
- 2) The characterization of the device will be performed in switching conditions and particularly for class E applications.
- 3) Very few components are needed to perform the extraction and thus, the error due to other component mismeasurements is small.

Non-linear large signal transistor models for simulation and design of high frequency circuits are, if available, often too complicated to be included in the theoretical design

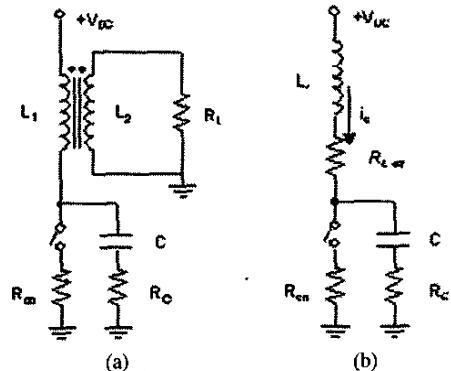


Fig. 1. (a) Class E simple circuit, (b) equivalent circuit of the simple class E network with only one inductor and one capacitor.

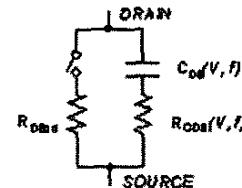


Fig. 2. Simple output port model for switching applications.

and analysis of class E amplifiers. The output port model considered in this paper (fig. 2) [2] is simple enough to be included in the analysis of a class E amplifier [3] but it also includes the output capacitance and the losses in the device both during cutoff and conduction. In this paper, a simple method, requiring no optimization process, will be demonstrated to characterize the model parameters from measurements.

II. EXACT ANALYSIS

The analytical description of the circuit presented in figure 1.b is based in the following assumptions:

- 1) The device has zero switching times, infinite OFF resistance and constant ON resistance.
- 2) The device has non-zero output capacitance that might be included in the circuit external shunt capacitance and

is independent of the device voltage (or it is a linear equivalent capacitance [3]). The shunt capacitance has a series loss resistance.

3) The L coil, has a series resistance that is included in the load equivalent.

According to the previous assumptions, the equivalent circuits for the OFF and the ON states are presented in figures 3a and 3b respectively¹. The device is driven at the input frequency, f , and the analysis will be performed in an interval, where $\theta = 2 \cdot \pi \cdot f \cdot t$, represents angular time. D is the duty cycle of the switching signal, thus $\theta_{ON} = 2 \cdot \pi \cdot D$ (instant of turn ON) and $\theta_{OFF} = 2 \cdot \pi \cdot (1 - D)$ (turn OFF)[4]. The differential equations, describing this two equivalent circuits are:

1) For the OFF state ($0 < \theta < 2 \cdot \pi \cdot D$)

$$(2\pi f)^2 \cdot L \cdot \frac{d^2 q(\theta)}{d\theta^2} + 2\pi f \cdot R_C \cdot \frac{dq(\theta)}{d\theta} + \frac{q(\theta)}{V_{DC}} = 0 \quad (1)$$

$$i_o(\theta) = 2\pi f \frac{dq(\theta)}{d\theta}$$

$$v_D(\theta) = R_C \cdot i_o(\theta) + \frac{q(\theta)}{V_{DC}}$$

2) For the ON state ($0 < \theta < 2 \cdot \pi \cdot (1 - D)$)

$$(2\pi f) \cdot L \cdot \frac{d^2 i'_o(\theta)}{d\theta^2} + (R_{on} + R_L) \cdot i'_o(\theta) = 0 \quad (2)$$

$$v_D(\theta) = R_C \cdot i'_o(\theta)$$

To solve the differential equations, that are initial conditions dependent, the following boundary conditions apply when the switch changes state:

$$i_o(2\pi D) = i'_o(0)$$

$$i'_o(2\pi(1 - D)) = i_o(0)$$

$$q(0) = 0$$

For class E operation [5], both the drain voltage, and the derivative of the voltage are set to be zero when the device turns ON, therefore:

$$v_D(2\pi D) = 0 \quad \xi = \frac{1}{V_{DC}} \cdot \frac{dv_D(\theta)}{d\theta} \Big|_{\theta=2\pi D} = 0 \quad (4)$$

Due to the simple structure of this circuit, the current flowing into the load is not a sinusoid and thus, the output harmonic content in the load resistance is not independent of the duty cycle chosen. To determine this relation the power supplied to the circuit has to be equal to the overall dissipated power in one cycle in the class E condition case where maximum efficiency occurs. To obtain this:

¹In the OFF equivalent circuit, the $R_C - C$ branch is ignored and the capacitor discharged to the source [2].

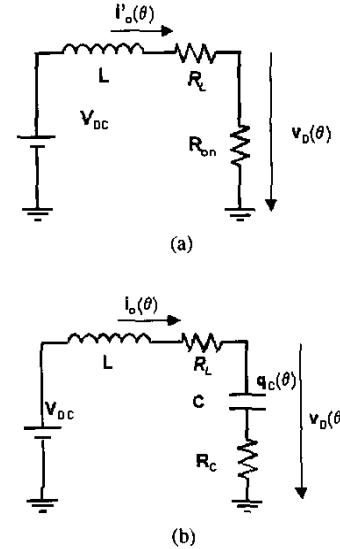


Fig. 3. (a) Equivalent circuit in ON, and (b) equivalent circuit in OFF.

$$P = V_{DC} \cdot I_{DC} = P_{load} + P_{diss} \quad (5)$$

$$I_{DC} = \frac{1}{2\pi} \int_0^{2\pi D} i_o(\theta) d\theta + \frac{1}{2\pi} \int_0^{2\pi(1-D)} i'_o(\theta) d\theta$$

$$P_{load} = \frac{R_L}{2\pi} \int_0^{2\pi D} i_o^2(\theta) d\theta + \frac{R_L}{2\pi} \int_0^{2\pi(1-D)} i'_o^2(\theta) d\theta \quad (6)$$

$$P_{diss} = \frac{R_C}{2\pi} \int_0^{2\pi D} i_o^2(\theta) d\theta + \frac{R_{on}}{2\pi} \int_0^{2\pi(1-D)} i'_o^2(\theta) d\theta$$

The maximum efficiency² depends on the dissipated power in the loss components. For this simple class E circuit that considers losses in the device, the efficiency can be expressed as:

$$\eta = \frac{P_{load}}{P_{dis}} = \frac{P_{DC} - P_{dis}}{P_{DC}} = 1 - \frac{P_{dis}}{P_{DC}} \quad (7)$$

The resulting equations (see Appendix) give by numerical solving the values of C , D and L provided that f , R_L (or, equivalently Q_L) and V_{DC} are known.

III. DEVICE MODEL AND CHARACTERIZATION

Figure 4 depicts the test circuit. If the device is substituted by the model, the resulting equations describing the circuit are equal to the ones derived before for both ON and OFF states. For this particular case:

²Efficiency is understood as overall efficiency and not first-harmonic power delivered to the load versus supply power. As it has been mentioned in the limitations of the circuit, for this simple circuit this ratio would be very poor.

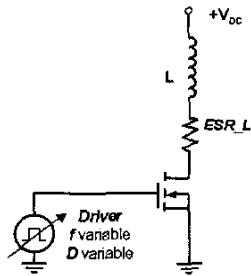


Fig. 4. Test circuit

- 1) There is no load resistor. Only the parasitic loss resistance of the coil, ESR_L , is present and it is assumed to be known.
- 2) No external capacitor is added, thus all the capacitance is provided by the device. The frequency and D are varied until ideal class E conditions are obtained. With the values of: f , D , L , ESR_L and V_{DC} , the equations (1) to (6) can be alternatively numerically solved to obtain the values of C , R_C and R_{on} and therefore extract the desired parameters.

The maximum frequency of operation of a device in the class E amplifier most common network with two inductors and two capacitors [4], [6] depends on the intrinsic output capacitance of the device. The maximum frequency in this case can be derived in terms of the linear equivalent capacitance [3], [7]:

$$f_{max} = \frac{1}{2} \cdot \left| \frac{\pi D \cos(\pi D) - \sin(\pi D)}{\frac{\pi D}{\sin(\pi D)}} \right| \cdot \frac{1}{\pi^2 R_L C_{eq}} \quad (8)$$

Thus the importance of knowing the exact value of C_{eq} . With the proposed method the linear equivalent capacitance is computed with no need for cumbersome curve fitting methods.

IV. EXPERIMENTAL VERIFICATION

A RF power MOSFET DE275-102N06A transistor has been tested. The experiment component values are presented in table I. The driver stage is based on an DEI EVIC420 evaluation board that permits switching frequencies up to 45MHz with variable amplitude and duty cycle. Table II shows

TABLE I
CIRCUIT VALUES FOR TEST SIMULATION

CLASS E CONDITIONS	
V_{DC}	20.4
L	347nH
ESR_L	4.56Ω
FREQUENCY	13.56 MHz
D	0.48
V_{PEAK}	75.6

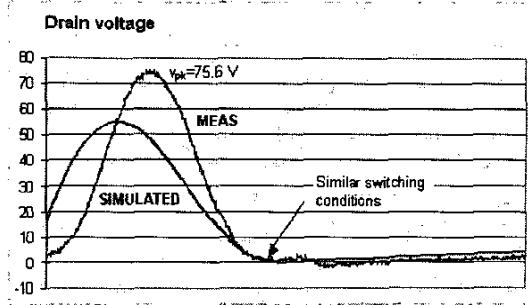


Fig. 5. Measured drain voltage vs. simulation with extracted parameters

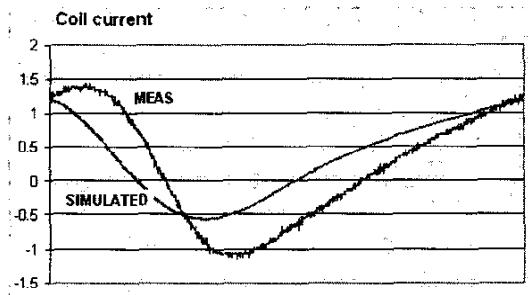


Fig. 6. Measured current vs. simulation with extracted parameters

the values of R_C , R_{ON} and C obtained by numerical solving of (1)-(6).

Fig. 5 depicts the drain voltage waveform compared to the simulated results with the extracted parameters. Switching conditions are equal in both cases but the peak voltage is higher than expected due to the non linearity of the output capacitance. The extracted value of C accounts for the linear equivalent capacitance defined in [2], [3]. Fig. 6 shows the current waveforms of the test circuit.

V. CONCLUSION

A method for the exact analysis and design of a very simple class E network, only with one capacitor and one inductor has been presented. This circuit has been applied to the parameter extraction of a switching device output port model particularly suited for designing class E applications. With this test a linear equivalent of the output capacitance of the device can easily be obtained and thus, the maximum frequency of operation of the device in regular class E applications can be computed.

TABLE II
EXTRACTED PARAMETERS

C	171.761pF
R_C	14.1Ω
R_{ON}	3.6Ω
V_{PEAK}	55.9V

Therefore, this method provides designers with a quick way to find out if a transistor will be useful in a class E application.

Laboratory results show good agreement with theoretical results obtained in terms of switching conditions. Further work by the authors would include a deeper discussion of the results of the simple class E design in terms of comparative graphs and the inclusion of the nonlinear output capacitance in the analysis.

For this particular case, the continuity equations given by (3) have explicit solution and thus:

$$i_o(0) = -\frac{\alpha \cdot \sin(\omega_1 \theta_{ON})(-J_1 \cdot K_1(1 - \alpha) - K_2)}{\alpha \beta K_1 \sin(\omega_1 \theta_{ON}) + \alpha \beta \cos(\omega_1 \theta_{ON}) - 1} + \dots$$

$$+ \frac{\alpha \cdot \cos(\omega_1 \theta_{ON}) J_1 \cdot (1 + \alpha)}{\alpha \beta K_1 \sin(\omega_1 \theta_{ON}) + \alpha \beta \cos(\omega_1 \theta_{ON}) - 1}$$

$$i'_o(0) = -\frac{J_1 - J_1 K_1 + K_2 \alpha \beta}{\alpha \beta K_1 \sin(\omega_1 \theta_{ON}) + \alpha \beta \cos(\omega_1 \theta_{ON}) - 1}$$

with

APPENDIX

This solution of the equations presented (1)-(6) applies for the general case of a couple pair of complex conjugate roots. This may not be the case for very high load values and/or very low Q .

1) For the OFF state ($0 < \theta < 2\pi D$)

$$q(\theta) = e^{-\sigma_{OFF}\theta} \cdot (C_1 \sin \omega_1 \theta + C_2 \cos \omega_1 \theta)$$

$$i_o(\theta) = e^{-\sigma_{OFF}\theta} \cdot (B_1 \sin \omega_1 \theta + B_2 \cos \omega_1 \theta)$$

$$v_D(\theta) = e^{-\sigma_{OFF}\theta} \cdot (M_1 \sin \omega_1 \theta + M_2 \cos \omega_1 \theta) + V_{DC}$$

with

$$C_1 = \frac{1}{2\pi f} \cdot \frac{i_o(0)}{\omega_1} - \frac{C V_{DC} \sigma_{OFF}}{\omega_1}$$

$$C_2 = -C \cdot V_{DC}$$

$$B_1 = 2\pi f (-\sigma_{OFF} \cdot C_1 - C_2 \cdot \omega_1)$$

$$B_2 = i_o(0)$$

$$M_1 = R_C \cdot B_1 + \frac{C_1}{C}$$

$$M_2 = R_C \cdot B_2 + \frac{C_2}{C}$$

$$\sigma_{OFF} = \frac{1}{2\pi f} \cdot \frac{R_L + R_C}{2L}$$

$$\omega_1 = \frac{1}{2\pi f} \sqrt{\frac{1}{LC} - \frac{(R_L + R_C)^2}{4L^2}}$$

2) For the ON state ($0 < \theta < 2\pi(1 - D)$)

$$i'_o(\theta) = J_1 + J_2 \cdot e^{-\sigma_{ON}\theta}$$

$$v'_D(\theta) = R_{ON} \cdot i'_o(\theta)$$

with

$$J_1 = \frac{V_{DC}}{R_L + R_{ON}}$$

$$J_2 = i'_o(0) - J_1$$

$$\sigma_{ON} = \frac{1}{2\pi f} \cdot \frac{R_L + R_{ON}}{L}$$

ACKNOWLEDGEMENT

This work was developed in the frame of a research project of the University of Zaragoza (Spain) in cooperation with the company OMB Sistemas Electrónicos S.A. (Zaragoza, Spain).

REFERENCES

- [1] N. O. Sokal, "Class E high-efficiency switching-mode tuned power amplifier with only one inductor and one capacitor in load network - approximate analysis," *IEEE Journal of Solid State Circuits*, vol. SC-16, no. 4, pp. 380-384, August 1981.
- [2] N. O. Sokal and R. Redl, "Power transistor output port model," *RF Design*, vol. 10, no. 6, pp. 45-48, 50, 51 and 53, June 1987.
- [3] A. Mediano, P. Molina, and J. Navarro, "Class E RF/microwave power amplifier: Linear "equivalent" of transistor's nonlinear output capacitance, normalized design and maximum operating frequency vs. output capacitance," in *Proc. Microwave Theory and Tech. Symposium*, Boston, 2000, pp. 783-786.
- [4] M. Albullet, "Analysis and design of the class E frequency multipliers with RF choke," *IEEE Transactions on Circuits and Systems-I: Fundamental Theory and Applications*, vol. 42, no. 2, pp. 95-104, February 1995.
- [5] N. O. Sokal and A. D. Sokal, "Class E - a new class of high-efficiency tuned single-ended switching power amplifiers," *IEEE Journal on Solid State Circuits*, vol. SC-10, No. 3, pp. 168-176, June 1975.
- [6] M. Kazimierczuk and K. Puczko, "Exact analysis of a class E tuned power amplifier at any Q and switch duty cycle," *IEEE Transactions on Circuits and Systems*, vol. CAS-34, no. 2, pp. 149-159, February 1987.
- [7] A. Mediano, "Contribución al estudio de los amplificadores de potencia de RF clase E. Influencia de la capacidad de salida del dispositivo activo," Ph.D. dissertation, University of Zaragoza (Spain), Department of Electronics and Communications Engineering, 1997, (in Spanish).